DN0002

Startup and Overshoot Design Solutions

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MP1580 DESIGN NOTE

Startup with a Slow Ramping Input Supply

Buck regulator products require under-voltage lockout to prevent the regulator from improper operation at very low input voltages. Also regulators require a minimum input voltage to enhance the main power switches. An issue can occur when the input voltage turns on very slowly and ramps through the under-voltage lockout threshold enabling the regulator output. The input voltage then falls back through the under-voltage lockout threshold as the regulator draws large input current. This trips the UVLO and the device shuts down. This will cause the output voltage to appear non-monotonic. The power regulator may oscillate back and forth around the under-voltage lockout threshold and cause the regulator output to droop. In the worst case, the regulator may never turn on if its output draws large current at startup.

The input capacitance of the regulator will hold up the input for:

$$\Delta T = \frac{(C \times \Delta V)}{I}$$

If ΔT is very long, then a very large capacitance is needed to keep the input from drooping. This is the case in a very slow power ramp up. See Figure 1 below:

Solution

The solution to the problem is to use the Enable pin as a programmable under-voltage lockout (UVLO) using a voltage divider from the input voltage of the regulator. This will allow the turn on of the regulator to be positioned much higher than the minimum input voltage. For example, the turn on threshold of a 5V input could be set for 4.75V, and that of a 12V input could be set for 9V. This will assure that the input voltage would be higher than the minimum input voltage for the device, and any voltage droop would not hit the minimum operating voltage of the device. Also, a larger input capacitor can be used when the supply is 5V, because 4.75V may only provide 0.5V headroom above the minimum input supply for the device.

The schematic shown in Figure 2 is a typical design with the programmable under-voltage lockout using a voltage divider. In this example, the input supply is nominally 12V and the output is 3.3V at 2A. The MP1580, a 2A buck regulator, is used in this design. It features a 380KHz switching frequency and a small SO8 package to enable a compact on board power solution. The UVLO programming resistors, R1 and R2, are chosen such to enable the regulator only after the input supply has reached 9V. The regulator will turn on when the EN pin reaches 2.495V at the input.

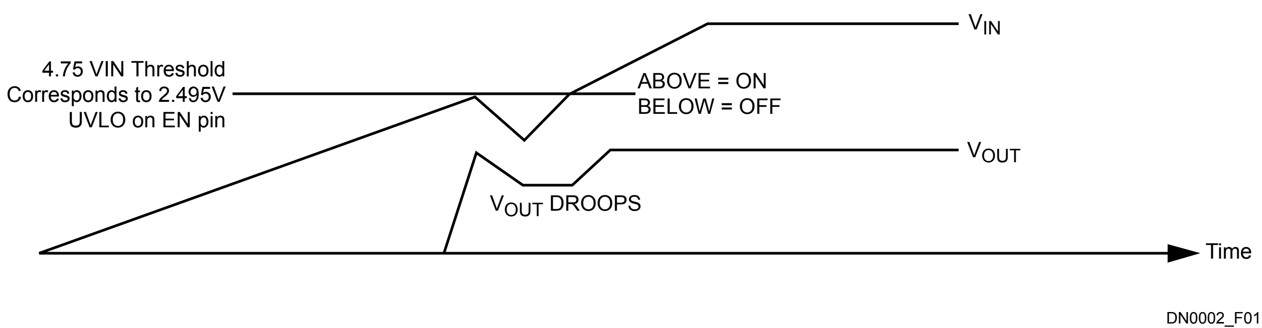

Figure 1—Slow Ramping V_{IN} vs. V_{OUT}

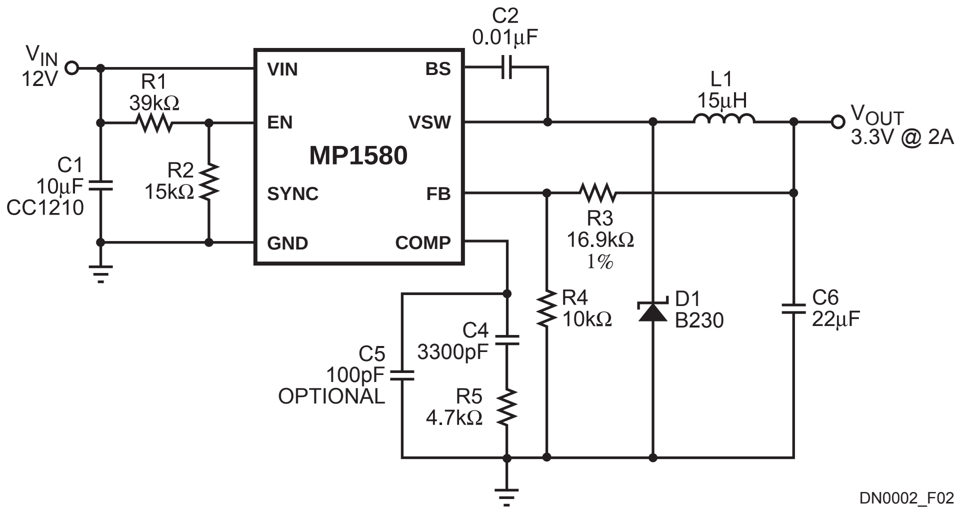

Figure 2—Voltage Divider for UVLO

MP1580 Overshoot Solutions

Some step down regulators can exhibit output voltage overshoot without a soft-start, or if the soft-start period is already over before the device is enabled due to power sequencing.

The MP1580 does not support the external soft-start. This may present an output overshoot problem if the output capacitor is too small. Careful design is required. This design note presents two solutions to address the overshoot problems.

Solution One

The MP1580 design shown in Figure 3 uses an external soft-start circuit to program the soft-start time; thus minimizing the turn-on overshoot.

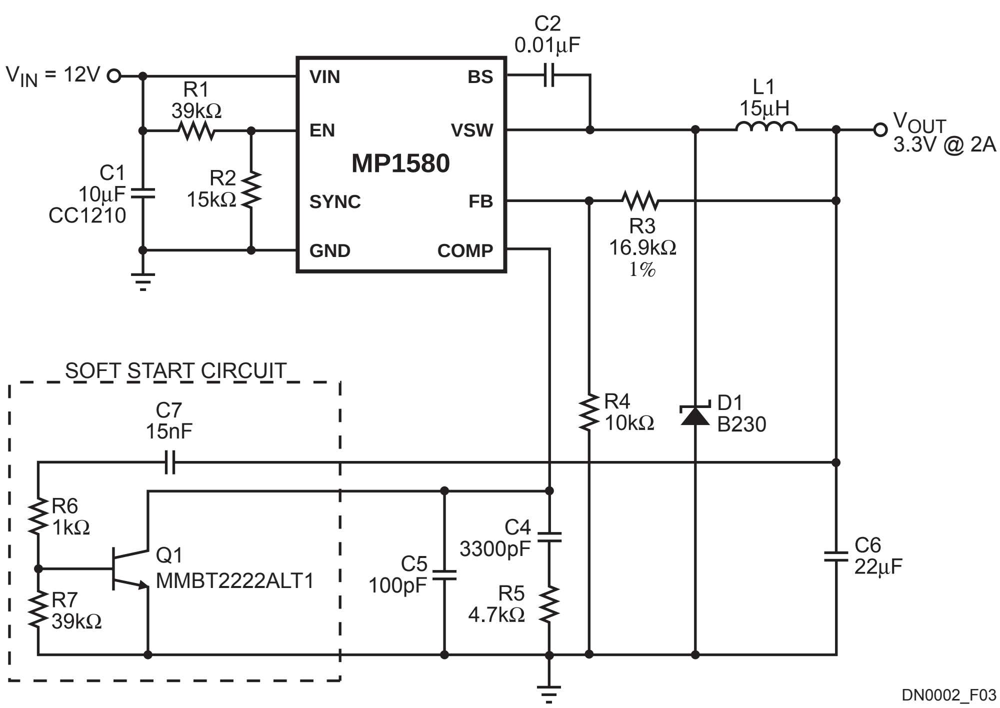

Figure 3—External Soft-Start Circuit

Components C7, R6, R7, and Q1 provide an output voltage controlled soft-start that servos the compensation pin to control output slew rate. The current into C7 is approximated as

$$I = \frac{C7 \times V_{OUT}}{RISETIME}$$

The current (I) will also be approximately equal to VBE / R7, since Q1 will turn on and control VOUT. The rise time is calculated as

$$RISETIME = \frac{(C7 \times V_{OUT} \times R7)}{V_{BE}}$$

The external component values shown in the example schematic of Figure 3 were chosen to produce a rise time of 1.5ms. The scope photo in Figure 4 below shows the controlled rise time of the output voltage.

Solution Two

The second solution is to provide an AC coupled feed-forward capacitor around the top feedback resistor to reduce the output overshoot. The example schematic in Figure 5 shows this design. The voltage divider on the EN pin for slow ramping power supplies is included as well. Both solutions can be used in parallel.

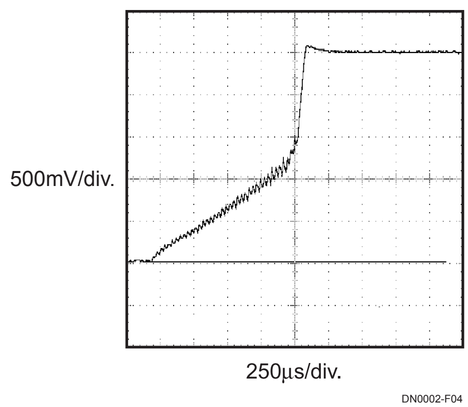

Figure 4—Output Voltage Ramp with External Soft-Start Circuit

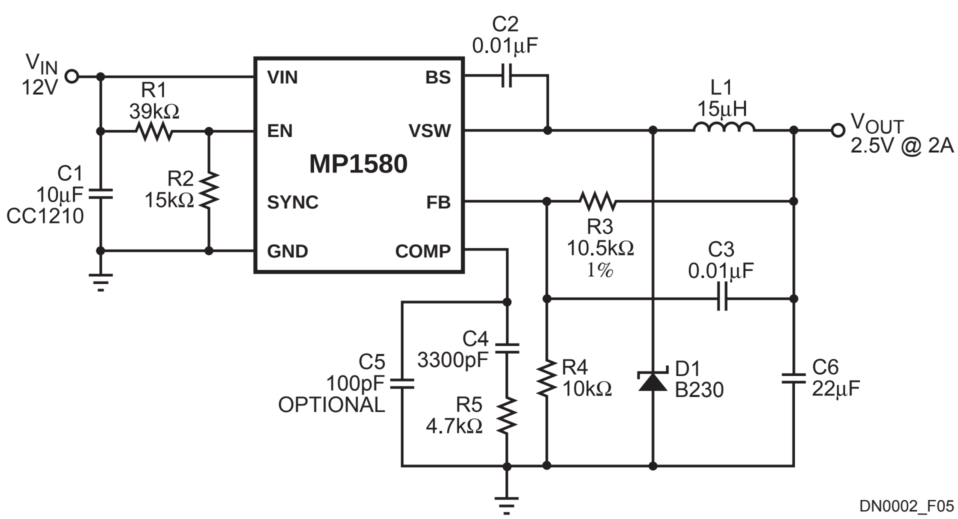

Figure 5—AC Coupled Feed-forward Feedback Loop

The output response is very controlled with instantaneous turn on. Figure 6 shows the turn on response.

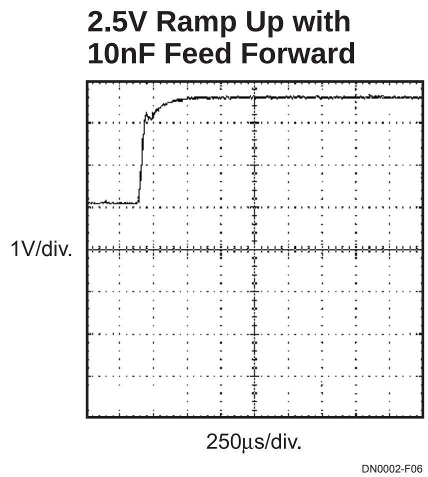

Figure 6—Output Voltage Ramp with External Soft-start Circuit

When using the feed-forward capacitor as in the above design, the stability of the regulator must be verified due to a possible change in the in the regulator's control loop response and phase margin. The analysis of the feedback loop with a spice model or a power supply control loop analyzer can verify the stability with the additional feed-forward capacitor. In addition, the transient response of the regulator can be checked with a fast step load generator to assure no oscillations are in the output response.

When the output voltage is close to the internal reference feedback voltage, the feed-forward capacitor method will lose its ability to resolve the output overshoot as the top feedback resistor becomes very small for lower output voltages and the feed-forward cap does not provide additional dynamic improvement. With the MP1580, the method may be less effective with output voltages < 1.8V. However, since the error amplifier will have more over-drive from the output and the closed loop gain will be much higher at low output voltages, these two factors will inherently reduce overshoot.

Figures 7 and 8 show the transient response and bode plot for the example schematic shown in Figure 5 with the 10nF feed-forward capacitor.

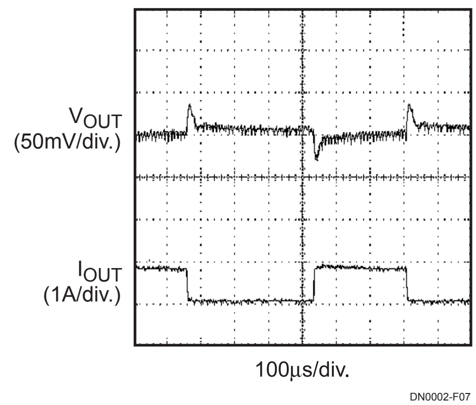

Figure 7—Output Voltage Transient Response with Feed-forward Capacitor

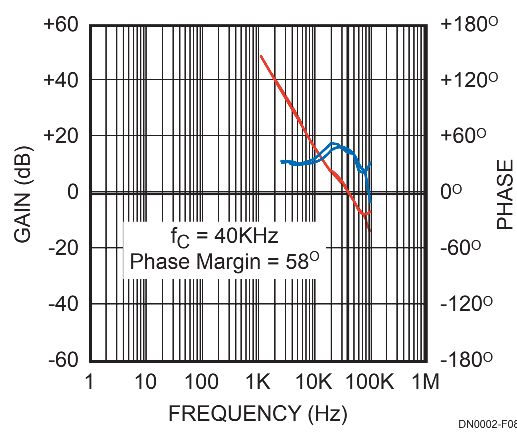

Figure 8—Bode Plot with Feed-forward Capacitor

The MP1580 is a current mode regulator, and many small signal spice model sources are available for these regulators. One of such websites is Ridley Engineering (www.ridleyengineering.com). Figure 9 shows a typical current mode regulator model for the MP1580.The following equations and notes are relevant to the above model.

EEout:

$$VALUE = \frac{V_{IN} \times \left(V(V_C, INN) - \frac{V_{OUT} \times R_S \times A_V}{R_{LOAD}} \right)}{V_P + \frac{(V_{IN} - V_{OUT}) \times R_S \times A_V}{(L \times F_S)}} + V_{OUT}$$

EAMP:

$$LAPLACE\left\{ \frac{s/F_S}{e^{\left(s/F_S\right)} - 1} \right\}$$

EES:

$$VALUE = V(I_{S+}, I_{S-}) \times A_V$$

G_M:

$$I = V(V_{REF}, F_B) \times G_M$$

Parameters:

PULSE(0 0.5 0 5µsec 5µsec 100µsec 200µsec 3)

V_{IN} = 12V

V_{OUT} = 2.5V

F_S = 380KHz

L = 15µH

R_S = 25mΩ

R_{LOAD} = 2.5Ω

G_M = 0.77millimhos

V_{REF} = 1.222V

A_V = 10

C_G = 5pF

R_G = 520kΩ

V_P = 100mV (slopecomp)

The schematic in Figure 5 is modeled and verified to the data taken in Figures 7 and 8. Please contact the MPS application group for any questions relating to these applications at 408-357-6600.

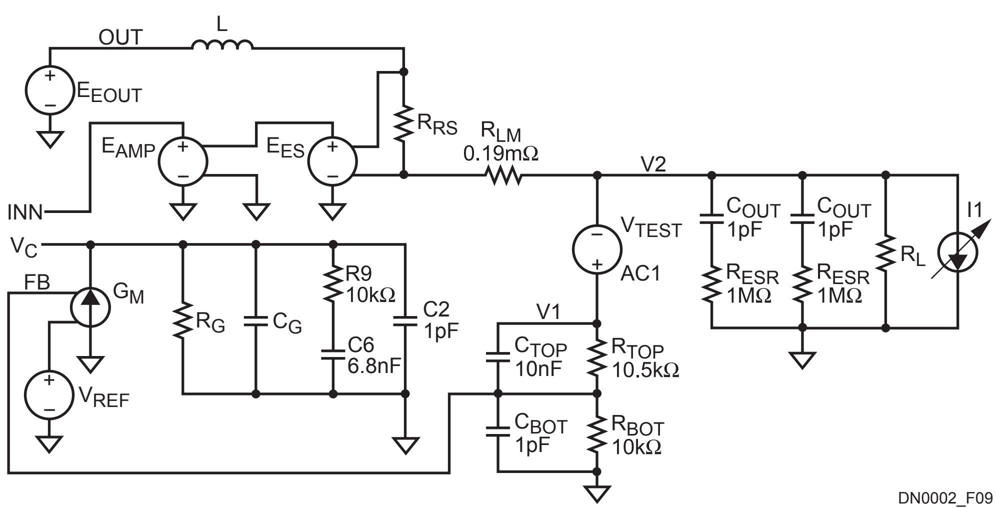

Figure 9—Current Mode Regulator Model